8085 code and output

1. 8 bit addition:

Code:

start: nop

LDA 8500

MOV B, A

LDA 8501

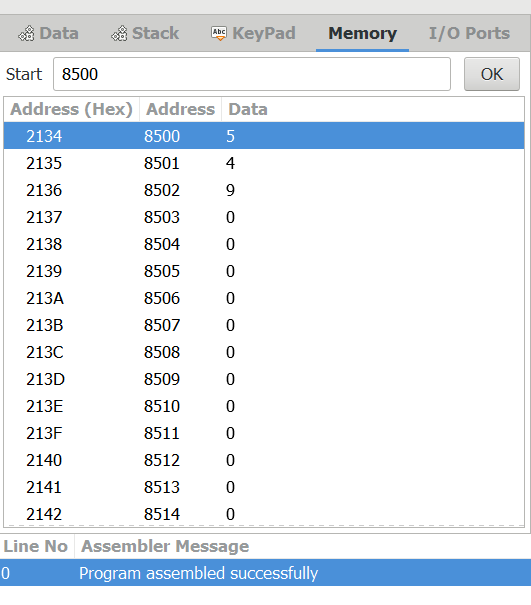
ADD B

STA 8502

RST 1

Hlt

Output:



1. 8 bit subtraction

Code:

start: nop

LDA 8000

MOV B, A

LDA 8001

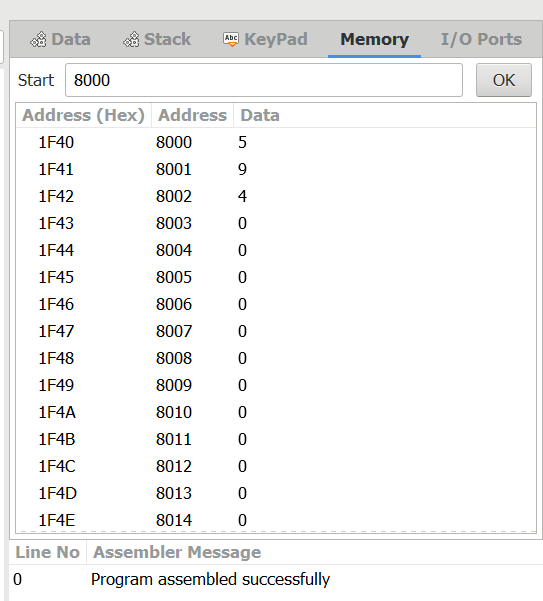
SUB B

STA 8002

RST 1

Hlt

Output:



1. 8 bit multiplication:

Code:

LDA 4200

MOV E,A

LDA 4202

MOV B,A

LXI H,0000H

MVI D,00H

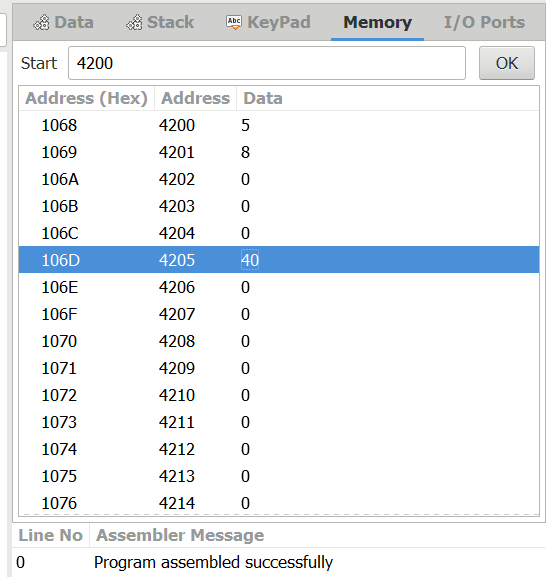
NEXT: DAD D

DCR B

JNZ NEXT

SHLD 4205H

Hlt



1. 8 bit division:

Code:

LDA 4201

MOV B,A

LDA 4200

MVI C,00H

AGAIN: CMP B

JC STORE

SUB B

INR C

JMP AGAIN

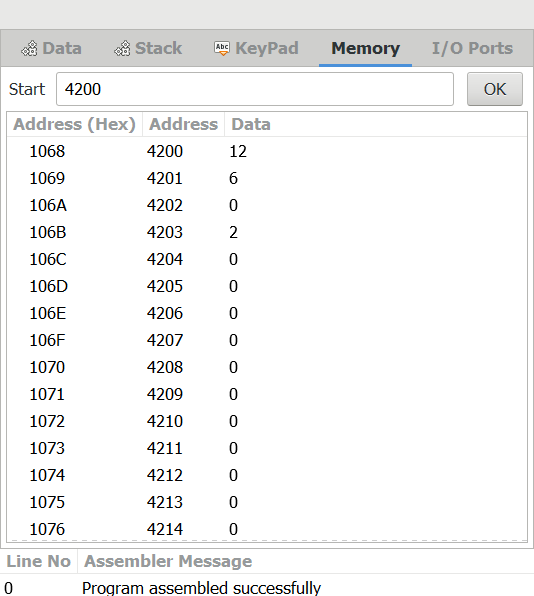
STORE: STA 4202

MOV A,C

STA 4203

Hlt

Output:



1. 16 bit addition:

Code:

LDA 3050

MOV B,A

LDA 3051

ADD B

STA 3052

LDA 3053

MOV B,A

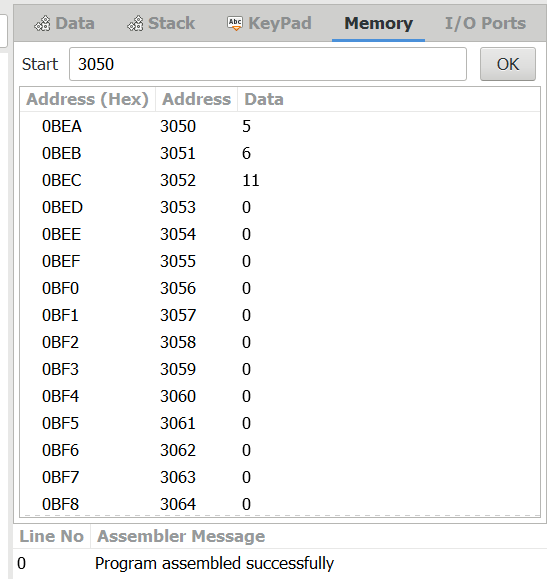
LDA 3054

ADC B

STA 3055

HLT

Output:



1. 16 bit subtraction:

Code:

LDA 3050

MOV B,A

LDA 3051

SUB B

STA 3052

LDA 3053

MOV B,A

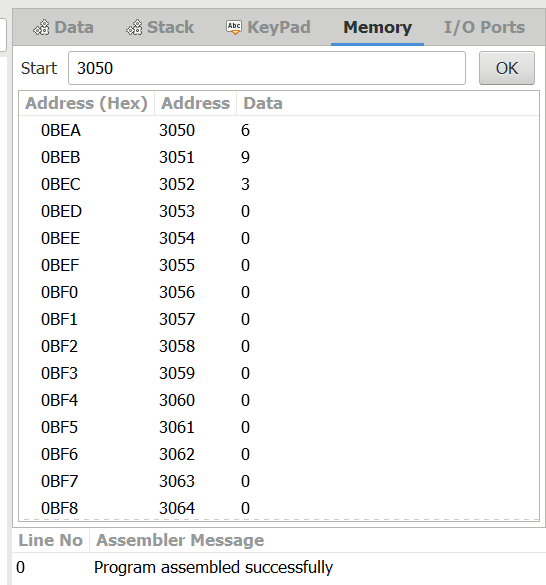
LDA 3054

SUB B

STA 3055

HLT

Output:



1. 16 bit multiplication:

Code:

LHLD 2050

SPHL

LHLD 2052

XCHG

LXI H,0000H

LXI B,0000H

AGAIN: DAD SP

JNC START

INX B

START: DCX D

MOV A,E

ORA D

JNZ AGAIN

SHLD 2054

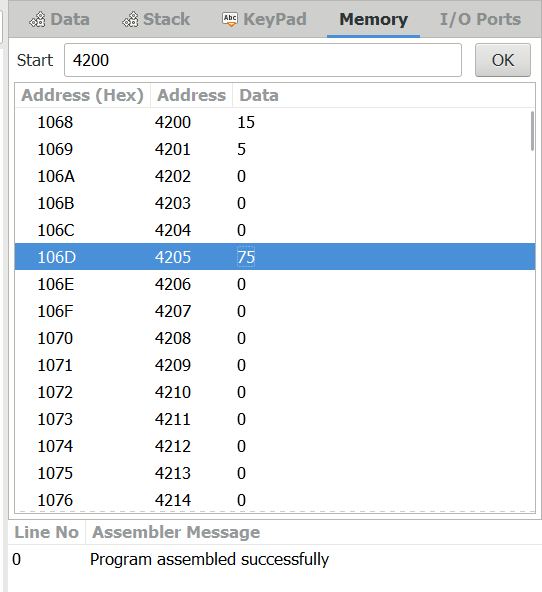
MOV L,C

MOV H,B

SHLD 2055

HLT

Output:



1. 16 bit division:

Code:

LDA 8501

MOV B,A

LDA 8500

MVI C,00

LOOP:CMP B

JC LOOP1

SUB B

INR C

JMP LOOP

STA 8503

DCR C

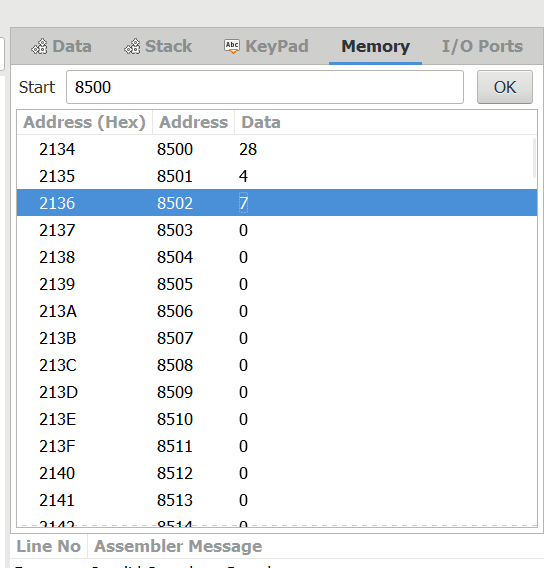
MOV A,C

LOOP1: STA 8502

RST 1

Hlt

Output:



1. Factorial:

Code:

LDA 2001

MOV B,A

MVI C,#01

MVI E,#01

LOOP: MOV D,C

MVI A,00H

LP: ADD E

DCR D

JNZ LP

MOV E,A

INR C

DCR B

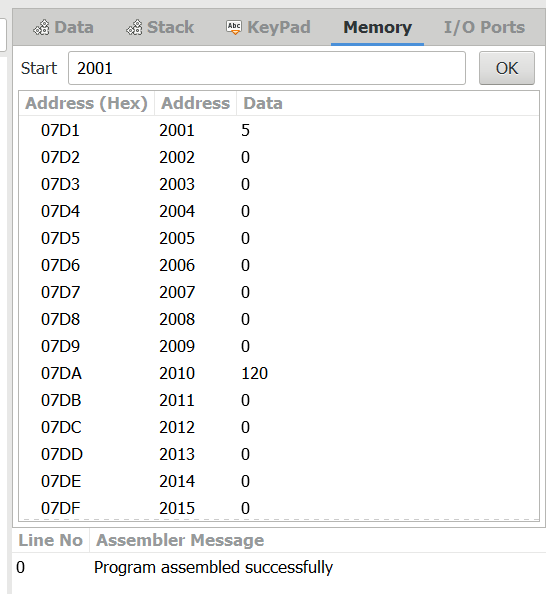
JNZ LOOP

MOV A,E

STA 2010

HLT

Output:



1. Largest number in array:

Code:

XI H,2050

MOV C,M

DCR C

INX H

MOV A,M

LOOP1: INX H

CMP M

JNC LOOP

MOV A,M

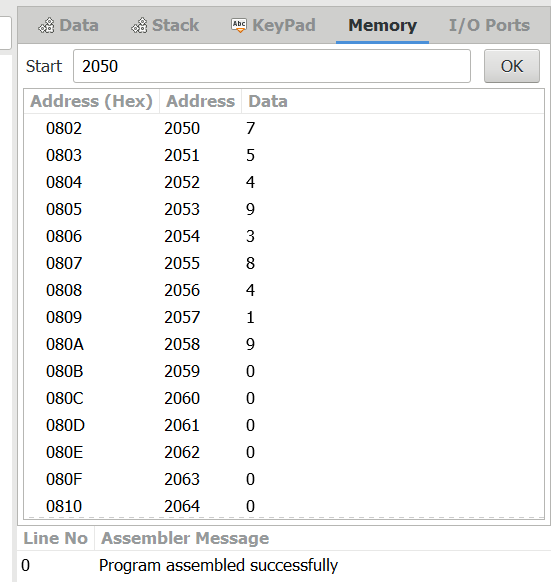
LOOP: DCR C

JNZ LOOP1

STA 2058

HLT

Output:



1. Smallest number in array:

Code:

LXI H,2050

MOV C,M

DCR C

INX H

MOV A,M

LOOP1: INX H

CMP M

JC LOOP

MOV A,M

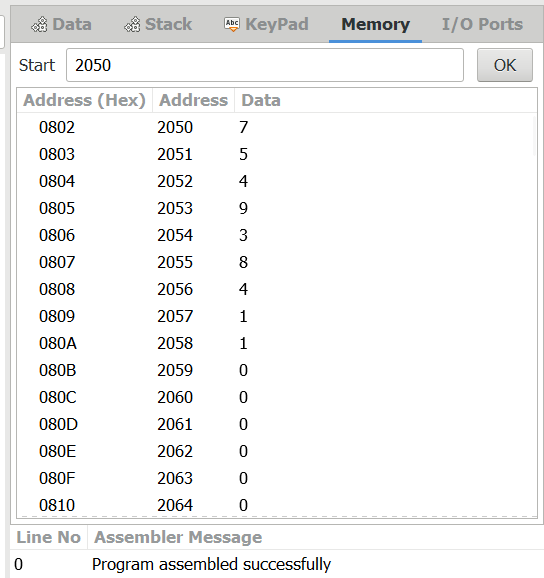
LOOP: DCR C

JNZ LOOP1

STA 2058

HLT

Output:



1. Ascending order:

Code:

LOOP: LXI H,3500

MVI D,00

MVI C,05

LOOP1: MOV A,M

INX H

CMP M

JC LOOP2

MOV B,M

MOV M,A

DCX H

MOV M,B

INX H

MVI D,01

LOOP2: DCR C

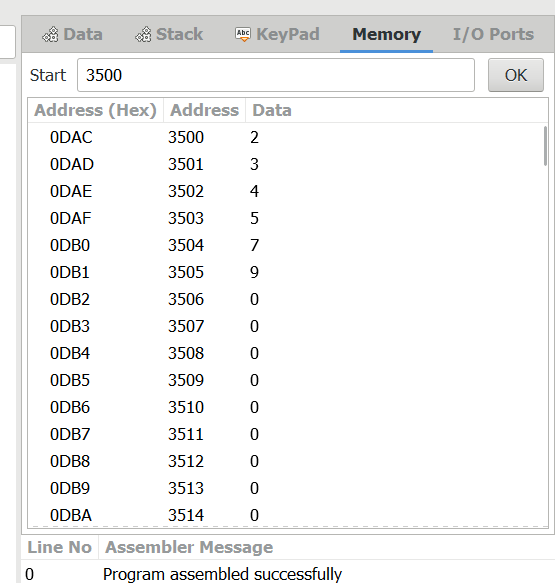
JNZ LOOP1

MOV A,D RRC

JC LOOP

HLT

Output:



1. Descending order:

Code:

LOOP: LXI H,3500

MVI D,00

MVI C,05

LOOP1: MOV A,M

INX H

CMP M

JNC LOOP2

MOV B,M

MOV M,A

DCX H

MOV M,B

INX H

MVI D,01

LOOP2: DCR C

JNZ LOOP1

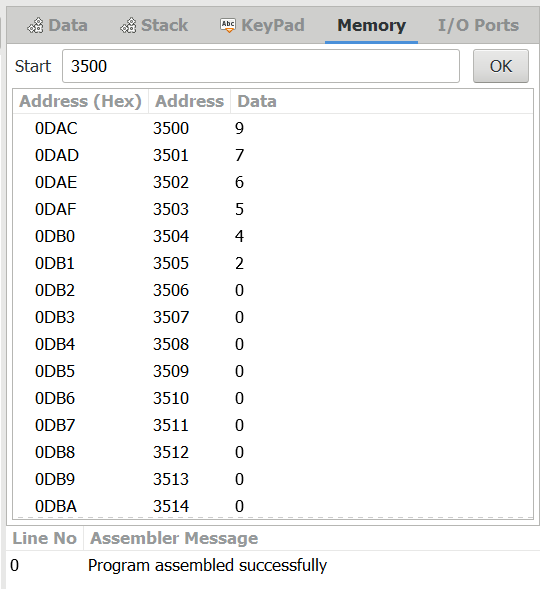
MOV A,D

RRC

JC LOOP

HLT

Output:



1. Addition of n numbers:

Code:

LXI H,8000

MOV C,M

MVI A,00

MOV B,A

LOOP: ADD C

JNC SKIP

INR B

SKIP: DCR C

JNZ LOOP

LXI H,8007

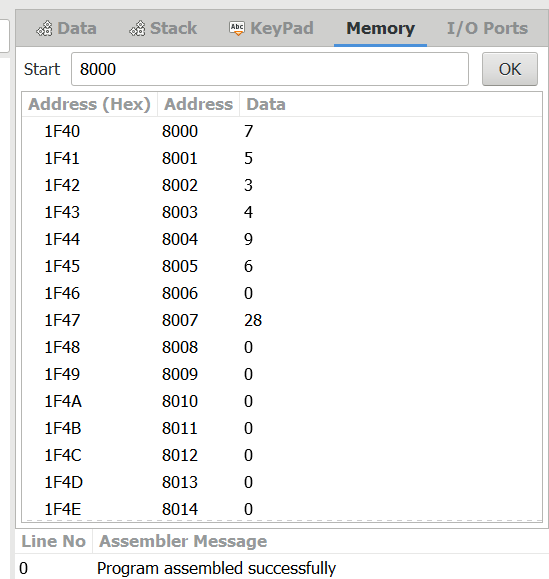
MOV M,A

INX H

MOV M,B

HLT

Output:



1. Swapping of numbers:

Code:

LDA 2001

MOV B,A

LDA 2002

MOV C,A

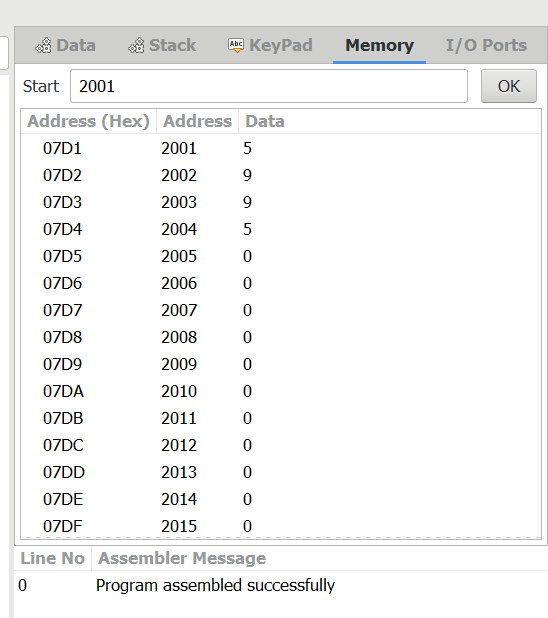
STA 2003

MOV A,B

STA 2004

HLT

Output:



1. Square of a number:

Code:

LXI H,8000

XRA A

MOV B,M

LOOP: ADD M

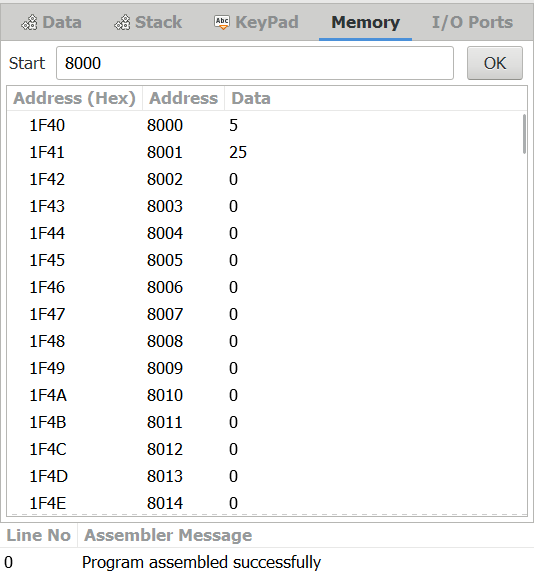
DCR B

JNZ LOOP

STA 8001

HLT

Output:



1. 1’s and 2’s complement :

Code:

LDA 3000

CMA

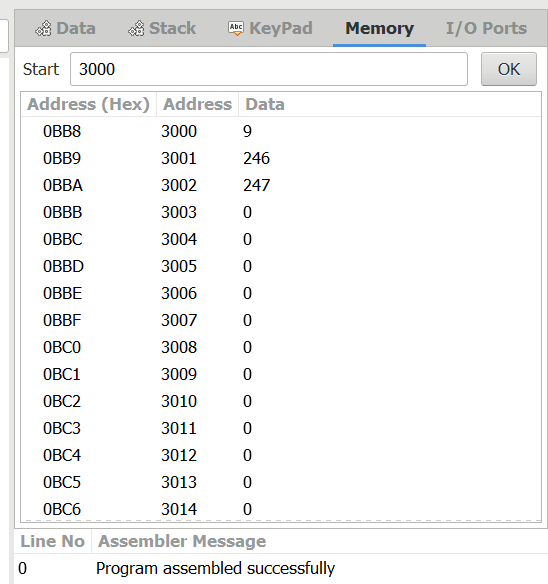
STA 3001

ADI 01

STA 3002

HLT

Output:



1. Rotate left operation:

Code:

MVI A,02

RLC

RLC

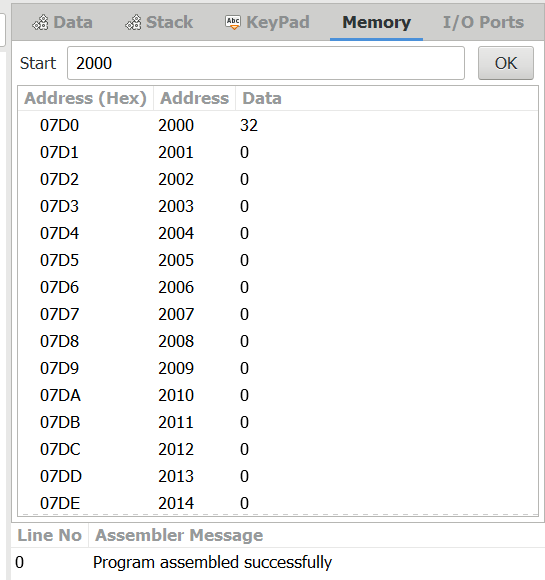
RLC

RLC

STA 2000

HLT

Output:



1. Rotate right operation:

Code:

MVI A,03

RRC

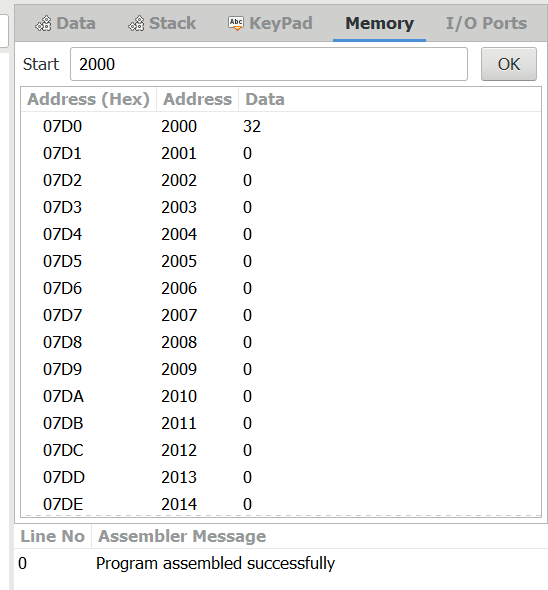
RRC

RRC

RRC

STA 2000

HLT



1. Logical operation:

Logical AND:

Code:

**AND OPERATION:**

MVI A,06

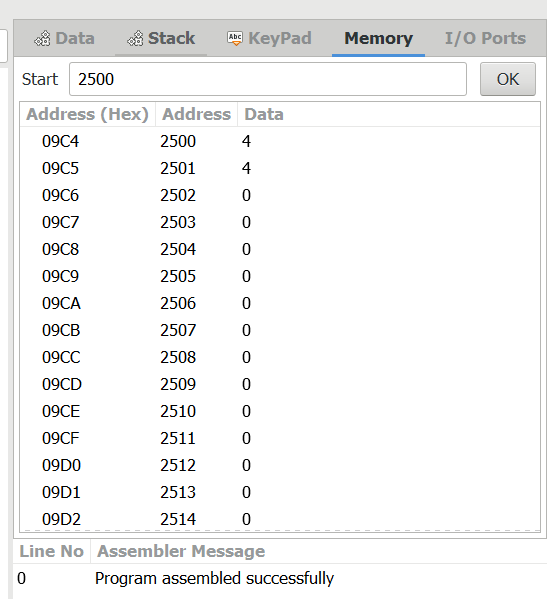
MVI B,04

ANA B

STA 2500

HLT

Output:



**OR OPERATION:**

MVI A,07

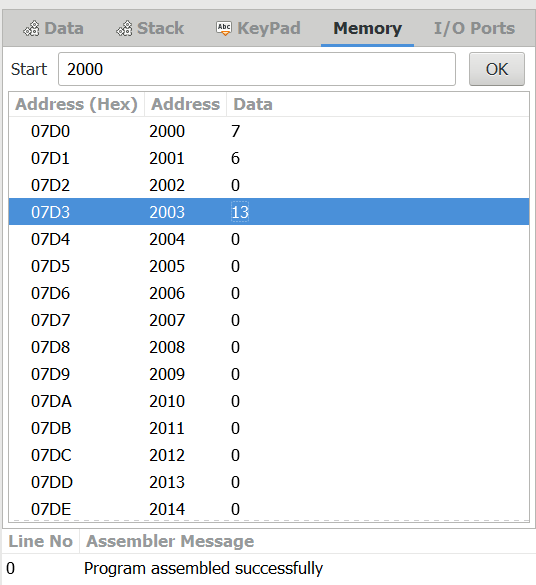
MVI B,06

ORA B

STA 2000

HLT

Output:



**XOR OPERATION:**

MVI A,03

MVI B,04

XRA B

STA 2000

HLT

Output:

